In the Claims:

1. (Currently Amended) A variable-gain digital filter having a construction in which a gain regulation circuit is incorporated inside the digital filter, said gain regulation circuit comprising: a first selector for selecting gain; and a first multiplier for directly multiplying ~~input data~~ a coefficient sequence with a gain signal~~, which is output of~~ that is outputted from said first selector.

2. (Currently Amended) A variable-gain digital filter according to claim 1 wherein:

said first multiplier of said gain regulation circuit multiplies ~~a~~ the gain signal that is outputted from said first selector with ~~a~~ the coefficient sequence that is switched and outputted from a second selector for each fixed time interval;

~~the~~ an output of said first multiplier is multiplied at a second multiplier with input data~~,~~ ~~that have been~~ said input data selected by a third selector that selects ~~and outputs~~ said input data from ~~each output~~ plural outputs of a shift register; and

~~the~~ an output of said second multiplier is then integrated by an integrator and outputted.

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3. (Currently Amended) A variable-gain digital filter comprising:

a shift register that is constituted by a plurality of stages of flip-flops and that both shifts input data and generates delayed output by each stage;

a first selector for selecting a gain;

a second selector for selecting a coefficient sequence;

a third selector for selecting each delay output of said shift register;

a first multiplier for multiplying an output of said first selector with an output of said second selector;

a second multiplier for multiplying an output of said first multiplier with an output of said third selector; and

an integrator for integrating an output of said second multiplier.

4. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are doubled in quantity ~~and makes each of them handles divided~~ to form two parts with each part handling one half of the delayed data; and

each of said first ~~to~~, second and third selectors ~~switch~~ switches output at each time interval of (T/n) × 2, where T is the duration of one time slot and n is ~~the~~ a filter order.

5. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are doubled in quantity ~~and~~ to form two parts, each part handling a half divided ~~loads half~~ load for each of said first to third selectors and said first and second multipliers; and

each of said first to third selectors ~~switch~~ switches output at each time interval of T/n, where T is the duration of one time slot and n is ~~the~~ a filter order.

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6. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are ~~increase~~ increased in quantity m times ~~in quantity to process each of them~~ to form m parts, each part handling only n/m delayed data allowing the processing speed of the first and second ~~multiplier~~ multipliers ~~for~~ to be 1/m where m is an integer greater than one and n is a filter order.

7. (Currently Amended) A variable-gain digital filter according to claim 3 wherein:

said first, second, and third selectors and said first and second multipliers are ~~increase~~ increased in quantity m times ~~in quantity to process each of them~~ to form m parts, each part handling only n/m delayed data to improve the processing speed of the variable-gain digital filter where m is an integer greater than one and n is a filter order.